

# **Foundations of VLSI Design and Circuit Implementation**

## **Chapter 1: Introduction to MOS Transistor**

1.1 MOS Transistor

1.2 CMOS Logic

1.3 Latches and Registers

1.4 Layout Design Rules

1.5 Stick Diagrams

1.6 Long Channel I-V Characteristics

1.7 C-V Characteristics

1.8 Non-Ideal I-V Effects

1.9 DC Transfer Characteristics

## **Chapter 2: Combinational MOS Logic Circuits**

2.1 Static CMOS

2.2 Dynamic CMOS

2.3 Cascade Voltage Switch Logic (CVSL)

2.4 Dynamic Circuits

2.5 Pass Transistor Logic

2.6 Transmission Gates

2.7 Domino and Dual Rail Domino Logic

2.8 Double Pass-Transistor Logic (DPL)

## **Chapter 3: Sequential Circuit Design**

3.1 Static Latches and Registers

3.2 Dynamic Latches and Registers

3.3 Pulse Registers

3.4 Sense Amplifier Based Register

3.5 Pipelining

3.6 Schmitt Trigger

3.7 Monostable Sequential Circuits

3.8 Astable Sequential Circuits

3.9 Timing Issues: Timing Classification of Digital System

3.10 Synchronous and Asynchronous Design

## **Chapter 4: Design of Arithmetic Building Blocks and Subsystem**

4.1 Data Paths

4.2 Adders

4.3 Multipliers

4.4 Shifters

4.5 ALUs

4.6 Signal Integrity Issues

4.7 Memory Architectures and Building Blocks

4.8 Designing Memory and Array Structures

4.9 Serial Access Memory

4.10 Low Power Memory Circuits

## **Chapter 5: Implementation Strategies and Testing**

5.1 FPGA Building Block Architectures, FPGA Interconnect Routing Procedures

5.2 Design for Testability: Ad Hoc Testing, Scan Design, BIST, IDDQ Testing, Design for Manufacturability, Boundary Scan

